AMENDMENTS TO THE CLAIMS

Kindly amend claims 1, 19, and 25 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An apparatus for performing cryptographic operations, comprising:

fetch logic, disposed within a microprocessor, configured to receive a cryptographic instruction~~, received by a microprocessor~~ as part of an instruction flow executing on said microprocessor, wherein said cryptographic instruction prescribes one of the cryptographic operations, and wherein said cryptographic instruction prescribes that an intermediate result be generated; and

execution logic, disposed within said microprocessor and operatively coupled to said cryptographic instruction, configured to execute said one of the cryptographic operations, and configured to generate said intermediate result.

2. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations further comprises:

an encryption operation, said encryption operation comprising encryption of one or more plaintext blocks to generate a corresponding one or more ciphertext blocks.

3. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations further comprises:

a decryption operation, said decryption operation comprising decryption of one or more ciphertext blocks to generate a corresponding one or more plaintext blocks.

4. (Original) The apparatus as recited in claim 1, wherein said execution logic is configured to interpret an intermediate result field within a control word which is referenced by said cryptographic instruction.

5. (Original) The apparatus as recited in claim 4, wherein said intermediate result field directs said execution logic to generate said intermediate result.

6. (Original) The apparatus as recited in claim 4, wherein said intermediate result field directs said execution logic to generate a normal result.

7. (Original) The apparatus as recited in claim 1, wherein said execution logic is configured to interpret a round count field within a control word which is referenced by said cryptographic instruction.

8. (Original) The apparatus as recited in claim 7, wherein the value of said round count field prescribes a number of cipher rounds to be performed on an input block during execution of said one of the cryptographic operations.

9. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations is accomplished according to the Advanced Encryption Standard (AES) algorithm.

10. (Previously Presented) The apparatus as recited in claim 1, wherein said cryptographic instruction is prescribed according to the instruction format for execution on an x86-compatible microprocessor.

11. (Original) The apparatus as recited in claim 1, wherein said cryptographic instruction implicitly references one or more registers within said computing device.

12. (Original) The apparatus as recited in claim 11, wherein said one or more registers comprises:

a first register, wherein contents of said first register comprise a first pointer to a first memory address, said first memory address specifying a first location in memory for access of one or more input text blocks upon which said one of the cryptographic operations is to be accomplished.

13. (Original) The apparatus as recited in claim 11, wherein said one or more registers comprises:

a second register, wherein contents of said second register comprise a second pointer to a second memory address, said second memory address specifying a second location in said memory for storage of a corresponding one or more output text blocks, said corresponding one or more output text blocks being generated as a result of accomplishing said one of the cryptographic operations upon one or more input text blocks.

14. (Original) The apparatus as recited in claim 11, wherein said one or more registers comprises:

a third register, wherein contents of said third register indicate a number of text blocks within one or more input text blocks.

15. (Original) The apparatus as recited in claim 11, wherein said one or more registers comprises:

a fourth register, wherein contents of said fourth register comprise a third pointer to a third memory address, said third memory address specifying a third location in memory for access of cryptographic key data for use in accomplishing said one of the cryptographic operations.

16. (Original) The apparatus as recited in claim 11, wherein said one or more registers comprises:

a fifth register, wherein contents of said fifth register comprise a fourth pointer to a fourth memory address, said fourth memory address specifying a fourth location in memory, said fourth location comprising a initialization vector location, contents of said initialization vector location comprising an initialization vector or initialization vector equivalent for use in accomplishing said one of the cryptographic operations.

17. (Original) The apparatus as recited in claim 11, wherein said one or more registers comprises:

a sixth register, wherein contents of said sixth register comprise a fifth pointer to a fifth memory address, said fifth memory address specifying a fifth location in memory for access of a control word for use in accomplishing said one of the cryptographic operations, wherein said control word prescribes cryptographic parameters for said one of the cryptographic operations, and wherein said control word comprises:

an intermediate result field, configured to specify whether a normal result or said intermediate result is to be generated during execution of said one of the cryptographic operations.

18. (Original) The apparatus as recited in claim 1, wherein said execution logic comprises:

a cryptography unit, configured execute a plurality of cryptographic rounds on each of one or more input text blocks to generate a corresponding each of one or more output text blocks, wherein said plurality of cryptographic rounds are prescribed by a round count field within a control word that is provided to said cryptography unit.

19. (Currently Amended) An apparatus for performing cryptographic operations, comprising:

a control word, configured to prescribe that an intermediate result be generated during execution of one of the cryptographic operations; and

a cryptography unit within a microprocessor, configured to execute said one of the cryptographic operations responsive to receipt of a cryptographic instruction within an instruction flow that prescribes said one of the cryptographic operations, wherein said cryptographic instruction is fetched from memory by fetch logic in said microprocessor, and wherein said cryptographic instruction also references said control word.

20. (Original) The apparatus as recited in claim 19, wherein said control word is stored in memory, and wherein a memory location of said control word is prescribed by contents of a register that is referenced by said cryptographic instruction.

21. (Original) The apparatus as recited in claim 19, wherein said cryptography unit executes said one of the cryptographic operations according to the Advanced Encryption Standard (AES) algorithm.

22. (Original) The apparatus as recited in claim 19, wherein said cryptography unit interprets an intermediate result field within said control word to determine whether to generate a normal result or said intermediate result.

23. (Original) The apparatus as recited in claim 19, wherein said cryptography unit interprets a round count field within said control word to determine how many block cipher rounds to execute on a block of input text during execution of said one of the cryptographic operations.

24. (Previously Presented) The apparatus as recited in claim 19, wherein said cryptographic instruction is prescribed according to the instruction format for execution on an x86-compatible microprocessor.

25. (Currently Amended) A method for performing cryptographic operations, comprising:

~~via a cryptographic~~within a microprocessor, fetching a cryptographic instruction from memory prescribing , ~~prescribing~~ that an intermediate result be generated during execution of one of a plurality of cryptographic operations; and

~~within a~~within the microprocessor, receiving the cryptographic instruction, and generating the intermediate result when executing the one of the cryptographic operations.

26. (Original) The method as recited in claim 25, wherein said prescribing comprises:

via a first field within a control word that is referenced by the cryptographic instruction, specifying whether a normal result or the intermediate result is to be generated.

27. (Original) The method as recited in claim 25, wherein said receiving comprises:

loading the control word from memory.

28. (Original) The method as recited in claim 25, said receiving comprises:

executing the one of the cryptographic operations according to the Advanced Encryption Standard (AES) algorithm.

29. (Previously Presented) The apparatus as recited in claim 22, wherein said prescribing comprises:

providing the cryptographic instruction according to the instruction format for execution on an x86-compatible microprocessor.

30. (Original) The method as recited in claim 25, wherein said prescribing comprises:

via a second field within a control word that is referenced by the cryptographic instruction, specifying how many cipher rounds are to be executed during execution of the one of the cryptographic operations on a block of input text.